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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/595,678

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Kazuki Noda

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05/12/2010

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EXAMINER

HENRY, CALEB E

ART UNIT

PAPER NUMBER

2894

NOTIFICATION DATE

DELIVERY MODE

05/12/2010

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/595,678	Applicant(s) NODA, KAZUKI	
	Examiner CALEB HENRY	Art Unit 2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 January 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

The amendments filed on 01/28/2010 have been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oka (6551906), in view of Farnworth (6180527).

Regarding claim 1, Oka teaches a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 3, lines 35-45), comprising in order:

joining the circuit side of said semiconductor wafer to a polymeric film material (Oka, fig. 1, 21) via a surface protecting layer (Oka, fig. 1, 22, UV curing resin/thermo-resin), and

grinding said wafer (Oka, col. 3, lines 45-48).

Oka does not teach the following (emphasis on the underlined and bold print):

joining the circuit side of said semiconductor wafer to a polymeric film material via a **fluid** surface protecting layer

hardening said surface protecting layer, and

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grinding said wafer,

wherein grinding said wafer is done after hardening said surface protecting layer.

Farnworth teaches a protection layer (Farnworth, fig. 1A-1C, 15,) used to protect a wafer (Farnworth, fig. 1A-1C, 13) during back grinding process, wherein this protective layer is **fluid** when applied to said wafer (Farnworth, col. 6, lines 32-35), is **hardened after being applied** to said wafer surface (Farnworth, col. 6, lines 35-49), **wherein grinding said wafer is done after hardening said surface protecting layer** (Farnworth, col. 5, lines 1-11).

Farnworth teaches that such a protective layer is cured when the temperature is elevated (thermosetting resin), when UV rays are used (UV curing resin), etc. Thus, it would be safe to assume that the UV curing resin in Oka could have these similar properties. Also, both layers are utilized as protecting layers during backgrinding process. It should be noted that Oka teaches using UV light to remove the UV resin after grinding. However, one with common knowledge in the art would know that when adhering UV resin to wafers, the resin is cured, **to a certain extent** (thus causing crosslinking to a certain extent). This is exemplified in Farnworth col. 6, lines 44-49 wherein it is taught that the resin is **cured to stage B, a partially cured non-tacky condition that occurs before all of the polymer is completely crosslinked, also known as an intermediate stage where the article is a green product.** One with common knowledge in the art would know that in order to peel the UV resin from the wafer, it is cured **past** the intermediate stage till the entire resin is crosslinked, allow it to be peeled off.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the said invention to append the teachings of Farnworth to the teachings of Oka due to aforementioned reasons.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka, in view of Farnworth, in further view of Kawate (6265460).

Regarding claim 2, Oka teaches a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 3, lines 35-45), comprising:

providing a surface protecting sheet comprising a polymeric film material (Oka, fig. 1A, 21) on which is a surface protecting layer (Oka, fig. 1A, 22, UV curing resin/thermo-resin), having a fluidizing temperature [**all resins, polymers, etc. have a fluidizing temperature**]

placing the circuit side of said semiconductor wafer (Oka, fig. 1A-1B, 1) in contact with the surface protecting layer (Oka, fig. 1A-1B),
grinding said wafer (Oka, col. 3, lines 45-48).

Oka does not teach the following (emphasis on the underlined and bold print):

providing a surface protecting sheet comprising a polymeric film material on which is a surface protecting layer, having a fluidizing temperature, and **which is solid at room temperature**

heating said surface protecting sheet to its fluidization temperature to make the surface protecting layer effectively fluid,

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placing the circuit side of said semiconductor wafer in contact with **the fluidized** surface protecting layer,

hardening said surface protecting layer upon exposure to radiation or upon heating to a temperature of 100°C or greater, and

grinding said wafer,

wherein grinding said wafer is done after hardening said surface protecting layer.

Farnworth teaches a protection layer (Farnworth, fig. 1A-1C, 15,) used to protect a wafer (Farnworth, fig. 1A-1C, 13) during back grinding process, wherein this protective layer is **fluid** when applied to said wafer (Farnworth, col. 6, lines 32-35), is **hardened after being applied** to said wafer surface (Farnworth, col. 6, lines 35-49), **wherein grinding said wafer is done after hardening said surface protecting layer** (Farnworth, col. 5, lines 1-11).

Farnworth teaches that such a protective layer is cured when the temperature is elevated (thermosetting resin), when UV rays are used (UV curing resin), etc. Thus, it would be safe to assume that the UV curing resin in Oka could have these similar properties. Also, both layers are utilized as protecting layers during backgrinding process. It should be noted that Oka teaches using UV light to remove the UV resin after grinding. However, one with common knowledge in the art would know that when adhering UV resin to wafers, the resin is cured, **to a certain extent** (thus causing crosslinking to a certain extent). This is exemplified in Farnworth col. 6, lines 44-49 wherein it is taught that the resin is **cured to stage B, a partially cured non-tacky condition that occurs before all of the polymer is completely crosslinked**, also

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known as an intermediate stage where the article is a green product. One with common knowledge in the art would know that in order to peel the UV resin from the wafer, it is cured **past** the intermediate stage till the entire resin is cross linked, allow it to be peeled off.

Kawate teaches the use of UV hot melt resins in IC packages wherein these resins **are solid at room temperature** (Kawate, col. 3, lines 66-67) but these same resins which are solid at room temperature **can be heated in order to liquefy them** (Kawate, col. 2, lines 50-52).

Kawate, like Farnworth and Oka, teaches the use of a UV resin in the semiconductor art. Also, Kawate teaches that by utilizing said resin, the resin will have improved flowability and thermal curability (Kawate, col. 3, lines 52-54).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the said invention to append the teachings of Farnworth and Kawate to the teachings of Oka due to aforementioned reasons.

Regarding claim 3, Oka/Farnworth/Kawate teach a surface protecting sheet for protection of the circuit side of a semiconductor wafer during the step of back side grinding of the wafer used in a method according to claim 2 (Oka, col. 3, lines 35-45).

Claims 4-6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka/Farnworth/Kawate as applied to claim 3 above, and further in view of Hosomi (5726219).

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Regarding claim 4, Oka/Farnworth/Kawate, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate, does not teach a surface protecting sheet according to claim 3, wherein, before hardening of the surface protective layer, the protective layer has an elastic shear loss modulus (G'') less than its elastic shear storage modulus (G') at room temperature (20-25°C) and an elastic shear loss modulus (G'') greater than its elastic shear storage modulus (G') at 30-100°C, as measured with a viscoelasticity measuring apparatus at a frequency of 10 Hz, a deformation of 0.04% and a temperature ramp rate of 3 °C/min., and the surface protective layer after hardening has an elastic tensile storage modulus (E') at 50°C greater than 5×10^7 Pa as measured with a viscoelasticity measuring apparatus at a frequency of 1 Hz, a deformation of 0.04% and a temperature-ramp rate of 5°C/min.

Hosomi teaches a resin which contains the components necessary to form phenol-novolac epoxy (meth)acrylate resin (Hosomi, col. 2, lines 25 -50, (b)). Since phenol-novolac epoxy (meth)acrylate resin is one of the main materials that can be utilized as the in the surface protecting layer, it must have the characteristics laid out in claim 4.

Hosomi teaches that phenol-novolac epoxy (meth)acrylate resin offers heat resistance at temperatures as high as 260 degrees Celsius. Also, these resins can be used as UV resins due to the fact that photo-polymerization initiators are added (Hosomi, col. 2, lines 25-50).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Farnworth/Kawate due to aforementioned reasons.

Regarding claim 5, Oka/Farnworth/Kawate teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate does not teach a surface protecting sheet according to claim 3, wherein the surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compound being:

(3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins.

Hosomi teaches a resin which contains the components necessary to form phenol-novolac epoxy (meth)acrylate resin (Hosomi, col. 2, lines 25 -50, (b)).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Farnworth/Kawate combination because phenol-novolac epoxy (meth)acrylate resin offers heat resistance at temperatures as high as 260 degrees Celsius.

Regarding claim 6, Oka/Farnworth/Kawate, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate, does not teach the use of a free-radical polymerization initiator.

Hosomi teaches the use of a free-radical polymerization initiator (photopolymerization initiator) (Hosomi, col. 2, lines 55-65, (e)).

Free-radical polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Farnworth/Kawate combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

Regarding claim 9, Oka/Farnworth/Kawate, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate, does not teach a surface protecting sheet according to claim 3, wherein the surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compound being:

(3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins.

Hosomi teaches a resin which contains the components necessary to form phenol-novolac epoxy (meth)acrylate resin (Hosomi, col. 2, lines 25 -50, (b)).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Farnworth/Kawate combination because phenol-novolac epoxy (meth)acrylate resin offers heat resistance at temperatures as high as 260 degrees Celsius.

Regarding claim 10, Oka/Farnworth/Kawate, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate, does not teach the use of a free-radical polymerization initiator.

Hosomi teaches the use of a free-radical polymerization initiator (photopolymerization initiator) (Hosomi, col. 2, lines 55-65, (e)).

Free-radical polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Hosomi to the teachings of the Oka/Farnworth/Kawate combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka/Farnworth/Kawate as applied to claim 3 above, and further in view of Komiyama (5118567).

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Regarding claim 7, Oka/Farnworth/Kawate, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate, does not teach a surface protecting sheet according to claim 3 wherein the surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the molecule, the cationically polymerizable compound being:

(2) phenol-novolac epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

Komiyama teaches the use of an adhesive tape which is composed of phenol-novolac epoxy resin (Komiyama, col. 3, lines 57-67). This adhesive tape has adhesive/releasing properties which are well balanced, which initially was a problem in prior art (Komiyama, col. 1, lines 30-36).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Farnworth/Kawate combination because it offers a balance between adhesive and releasing properties.

Regarding claim 8 Oka/Farnworth/Kawate, teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate, does not teach the use of a free-radical polymerization initiator.

Komiyama teaches the use of a cationic polymerization initiator (photopolymerization initiator) (Komiyama, col. 2, lines 1-12).

Cationic polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Farnworth/Kawate combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka/Farnworth/Kawate/Hosomi as applied to claim 4 above, and further in view of Komiyama (5118567).

Regarding claim 11 Oka/Farnworth/Kawate/Hosomi teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate/Hosomi do not teach a surface protecting sheet according to claim 3 wherein the surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the molecule, the cationically polymerizable compound being:
(2) phenol-novolac epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

Komiyama teaches the use of an adhesive tape which is composed of phenol-novolac epoxy resin (Komiyama, col. 3, lines 57-67). This adhesive tape has adhesive/releasing properties which are well balanced, which initially was a problem in prior art (Komiyama, col. 1, lines 30-36).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Farnworth/Kawate/Hosomi combination because it offers a balance between adhesive and releasing properties.

Regarding claim 12, Oka/Farnworth/Kawate/Hosomi teach a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer (Oka, col. 2, lines 55-65).

Oka/Farnworth/Kawate/Hosomi does not teach the use of a free-radical polymerization initiator.

Komiyama teaches the use of a cationic polymerization initiator (photopolymerization initiator) (Komiyama, col. 2, lines 1-12).

Cationic polymerization initiators are needed in UV curing resin in order to initiate polymerization reaction.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to append the teachings of Komiyama to the teachings of the Oka/Farnworth/Kawate/Hosomi combination because UV curing resins generally need a free-radical polymerization initiator in order for the UV light to have its intended effect.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection. Please see above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALEB HENRY whose telephone number is (571)270-5370. The examiner can normally be reached on 9 a.m.-5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CALEB HENRY/
Examiner, Art Unit 2894

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art
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